ECE4250 Lab 3

State Machine

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# Objective

The Objective of this lab was to set up the test bench to test a VHDL design. In this lab, we used the 6-bit subtractor as the test design. The test bench used a golden vector for testing outputs.

# Lab Work

Referencing example 2-68 on page 104 of the textbook, we implemented a similar test bench with 5 test inputs all referencing the golden vectors for the testing. Using the 6-bit full subtractor from lab 2. Since we already had confirmed the subtractor worked, the first test bench run verified that result. The successful output was simply “Test Finished.” To test the test bench was working properly, one of the golden vectors was changed to be incorrect. Running the test after that produced “Wrong answer when subtracting iteration” messages with the clock time for the incorrect vector.

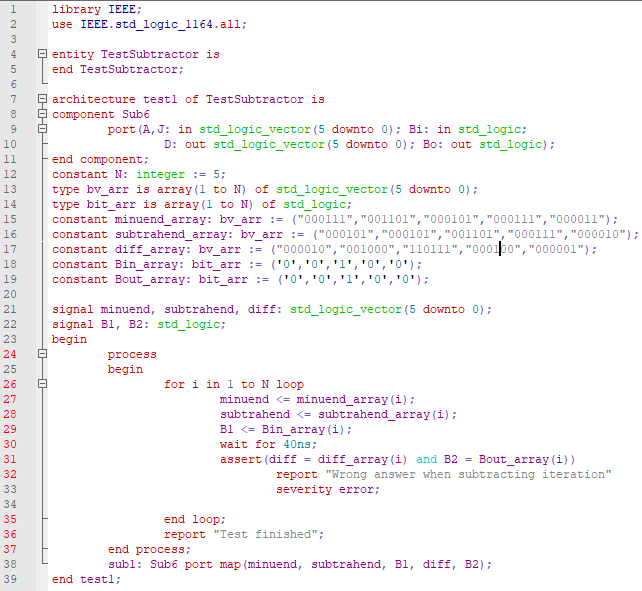


Figure . Test bench code

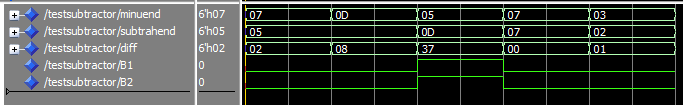


Figure . Correct simulation results

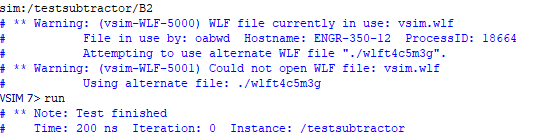


Figure . Correct simulation output

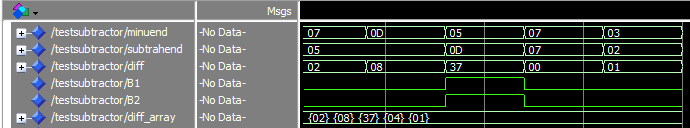


Figure . Failed simulation results, 4th golden vector changed to 04 instead of 00

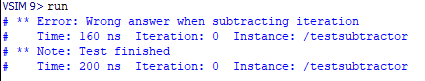


Figure . Failed simulation outputs

# Conclusion

Adapting the 4-bit adder test bench example was simple as it just required changing some vectors and connecting the appropriate subtractors in place of the adders. The only issues I had were from mismatched variables between the test bench, subtractor, and 6-bit subtractor since it appears, I had the wrong files from lab 2 saved. After renaming a few signals, and correcting the subtractor files, the test bench successfully executed with the correct golden vector.

Reference:

C. H. Roth, L. K. John. “Introduction to VHDL,” in *Digital System Design Using VHDL*. 3rd Ed. Boston MA, United States: Cengage, 2016, ch. 2.